What is claimed is:

1. A computer system comprising:

a central processing unit;

a plurality of peripheral devices operatively associated with said central processing unit and comprising volatile memory, non-volatile memory, and a plurality of I/O subsystems to and from which data flows are exchanged with said central processor for processing of data by said central processing unit; and

a network processor operatively interposed between said central processing unit and said peripheral devices and among said peripheral devices, said network processor having

a plurality of interface processors;

instruction memory storing instructions accessibly to said interface processors;

data memory storing accessibly to said interface processors data passing through said network processor from and to said peripheral devices; and

a plurality of input/output ports exchanging data passing through said network processor with said peripheral devices;

said network processor cooperating with said central processing unit in directing the exchange of data between said input/output ports and the flow of data through said data memory to and from said volatile memory and said non-volatile memory in response to execution by said interface processors of instructions loaded into said instruction memory.

2. Apparatus according to Claim 1 wherein said network processor comprises a semiconductor substrate and further wherein said interface processors, said instruction memory, said data memory and said input/output ports are formed on said semiconductor substrate.

3. Apparatus according to Claim 1 wherein the number of said interface processors exceeds four.

4. Apparatus according to Claim 1 wherein one of said input/output ports is operatively connected with each corresponding one of said plurality of I/O subsystems.

5. A method comprising the steps of:

passing bit streams of data moving within a computer system to and from a central processing unit through a network processor;

passing bit streams of data moving within the computer system to and from peripheral devices operatively associated with the central processing unit through the network processor; and

processing and translating virtual and physical memory addresses for the bit streams at the network processor.

6. A method according to Claim 5 wherein the step of processing addresses comprises broadcasting bit streams to a plurality of devices.